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 Zhiguo Ge; Weng-Fai Wong; Hock-Beng Lim;
Design, Automation & Test in Europe Conference & Exhibition, 2007. DATE '07
 16-20 April 2007 Page(s):1 - 6
 Digital Object Identifier 10.1109/DATE.2007.364484
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- ☐ **2. Memory hierarchy layer assignment for data re-use exploitation in multimedia algorithms realized on predefined processor architectures**
 Masselos, K.; Catthoor, F.; Kakarudas, A.; Goutis, C.E.; De Man, H.;
Electronics, Circuits and Systems, 2001. ICECS 2001. The 8th IEEE International Conference on
 Volume 1, 2-5 Sept. 2001 Page(s):285 - 288 vol.1
 Digital Object Identifier 10.1109/ICECS.2001.957735
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- ☐ **3. Memory hierarchy considerations for cost-effective cluster computing**
 Xing Du; Xiaodong Zhang; Zhichun Zhu;
Computers, IEEE Transactions on
 Volume 49, Issue 9, Sept. 2000 Page(s):915 - 933
 Digital Object Identifier 10.1109/12.869323
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(540 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- ☐ **4. Towards virtually-addressed memory hierarchies**
 Xiaogang Qiu; Dubois, M.;
High-Performance Computer Architecture, 2001. HPCA. The Seventh International Symposium on
 19-24 Jan. 2001 Page(s):51 - 62
 Digital Object Identifier 10.1109/HPCA.2001.903251
[AbstractPlus](#) | Full Text: [PDF\(1004 KB\)](#) IEEE CNF
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- ☐ **5. The impact of memory hierarchies on cluster computing**
 Xing Du; Xiaodong Zhang;
[Parallel and Distributed Processing, 1999. 13th International and 10th Symposium on Parallel and Distributed Processing, 1999. 1999 IPPS/SPDP. Proceedings](#)
 12-16 April 1999 Page(s):61 - 69
 Digital Object Identifier 10.1109/IPPS.1999.760435
[AbstractPlus](#) | [Full Text: PDF\(288 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)
-
- ☐ **6. A Decoupled Architecture of Processors with Scratch-Pad Memory Hierarchy**
 Milidonis, A.; Alachiotis, N.; Porpodas, V.; Michail, H.; Kakarountas, A.P.; Goutis, C.E.;
[Design, Automation & Test in Europe Conference & Exhibition, 2007. DATE '07](#)
 16-20 April 2007 Page(s):1 - 6
 Digital Object Identifier 10.1109/DATE.2007.364661
[AbstractPlus](#) | [Full Text: PDF\(173 KB\)](#) [IEEE CNF](#)
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-
- ☐ **7. A reconfigurable instruction memory hierarchy for embedded systems**
 Zhiguo Ge; Hock Beng Lim; Weng Fai Wong;
[Field Programmable Logic and Applications, 2005. International Conference on](#)
 24-26 Aug. 2005 Page(s):7 - 12
 Digital Object Identifier 10.1109/FPL.2005.1515691
[AbstractPlus](#) | [Full Text: PDF\(259 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)
-
- ☐ **8. Compiler-directed scratch pad memory hierarchy design and management**
 Kandemir, M.; Choudhary, A.;
[Design Automation Conference, 2002. Proceedings. 39th](#)
 10-14 June 2002 Page(s):628 - 633
 Digital Object Identifier 10.1109/DAC.2002.1012701
[AbstractPlus](#) | [Full Text: PDF\(814 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)
-
- ☐ **9. A concurrent hardware software management scheme for memory hierarchies**
 Hammami, O.;
[Industrial Electronics, 1994. Symposium Proceedings. ISIE '94., 1994 IEEE International Symposium on](#)
 25-27 May 1994 Page(s):368 - 373
 Digital Object Identifier 10.1109/ISIE.1994.333088
[AbstractPlus](#) | [Full Text: PDF\(580 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)
-
- ☐ **10. Hardware/software co-synthesis with memory hierarchies**
 Yanbing Li; Wolf, W.H.;
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)
 Volume 18, [Issue 10](#), Oct. 1999 Page(s):1405 - 1417
 Digital Object Identifier 10.1109/43.790618
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(268 KB\)](#) [IEEE JNL](#)
[Rights and Permissions](#)
-
- ☐ **11. Bit-Width Constrained Memory Hierarchy Optimization for Real-Time Video Systems**
 Thornberg, B.; Palkovic, M.; Qubo Hu; Olsson, L.; Kjeldsberg, P.G.; O'Nils, M.; Catthoor, F.;
[Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on](#)
 Volume 26, [Issue 4](#), April 2007 Page(s):781 - 800
 Digital Object Identifier 10.1109/TCAD.2006.884569
[AbstractPlus](#) | [Full Text: PDF\(1359 KB\)](#) [IEEE JNL](#)
[Rights and Permissions](#)
-

- ☐ **12. MSCSim -Multilevel and Split Cache Simulator**
 Coutinho, L.M.N.; Mendes, J.L.D.; Martins, C.A.P.S.;
[Frontiers in Education Conference, 36th Annual](#)
 Oct. 2006 Page(s):7 - 12
 Digital Object Identifier 10.1109/FIE.2006.322536
[AbstractPlus](#) | Full Text: [PDF\(948 KB\)](#) IEEE CNF
[Rights and Permissions](#)
-
- ☐ **13. The cost of cache-oblivious searching**
 Bender, M.A.; Brodal, G.S.; Fagerberg, R.; Ge, D.; Simai He; Haodung Hu; Iacono, J.; Lopez-Ortiz, A.;
[Foundations of Computer Science, 2003. Proceedings. 44th Annual IEEE Symposium on](#)
 11-14 Oct. 2003 Page(s):271 - 282
[AbstractPlus](#) | Full Text: [PDF\(387 KB\)](#) IEEE CNF
[Rights and Permissions](#)
-
- ☐ **14. Memory hierarchy reconfiguration for energy and performance in general-purpose processor architectures**
 Balasubramonian, R.; Albones, D.; Buyuktosunoglu, A.; Dwarkadas, S.;
[Microarchitecture, 2000. MICRO-33. Proceedings. 33rd Annual IEEE/ACM International Symposium on](#)
 10-13 Dec. 2000 Page(s):245 - 257
 Digital Object Identifier 10.1109/MICRO.2000.898075
[AbstractPlus](#) | Full Text: [PDF\(1128 KB\)](#) IEEE CNF
[Rights and Permissions](#)
-
- ☐ **15. Memory Hierarchy Targeting Bi-Predictive Motion Compensation for H.264/AVC Decoder**
 Zatt, B.; Azevedo, A.; Agostini, L.; Susin, A.; Bampi, S.;
[VLSI, 2007. ISVLSI '07. IEEE Computer Society Annual Symposium on](#)
 9-11 March 2007 Page(s):445 - 446
 Digital Object Identifier 10.1109/ISVLSI.2007.64
[AbstractPlus](#) | Full Text: [PDF\(187 KB\)](#) IEEE CNF
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-
- ☐ **16. Using a victim buffer in an application-specific memory hierarchy**
 Chuanjun Zhang; Vahid, F.;
[Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings](#)
 Volume 1, 16-20 Feb. 2004 Page(s):220 - 225 Vol.1
 Digital Object Identifier 10.1109/DATE.2004.1268852
[AbstractPlus](#) | Full Text: [PDF\(234 KB\)](#) IEEE CNF
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-
- ☐ **17. Memory hierarchy considerations for fast transpose and bit-reversals**
 Gatlin, K.S.; Carter, L.;
[High-Performance Computer Architecture, 1999. Proceedings. Fifth International Symposium On](#)
 9-13 Jan. 1999 Page(s):33 - 42
 Digital Object Identifier 10.1109/HPCA.1999.744320
[AbstractPlus](#) | Full Text: [PDF\(176 KB\)](#) IEEE CNF
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-
- ☐ **18. Performance improvement of the memory hierarchy of RISC-systems by application of 3-D-technology**
 Kleiner, M.B.; Kuhn, S.A.; Weber, W.;
[Electronic Components and Technology Conference, 1995. Proceedings., 45th](#)
 21-24 May 1995 Page(s):645 - 655
 Digital Object Identifier 10.1109/ECTC.1995.515351
[AbstractPlus](#) | Full Text: [PDF\(1024 KB\)](#) IEEE CNF
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-

- ☐ **19. Modeling parallel computers as memory hierarchies**
 Alpern, B.; Carter, L.; Ferrante, J.;
[Programming Models for Massively Parallel Computers, 1993. Proceedings](#)
 20-23 Sept. 1993 Page(s):116 - 123
 Digital Object Identifier 10.1109/PMMP.1993.315548
[AbstractPlus](#) | [Full Text: PDF\(548 KB\)](#) [IEEE CNF](#)
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-
- ☐ **20. Memory Hierarchy Configuration Analysis**
 Welch, T.A.;
[Computers, IEEE Transactions on](#)
 Volume C-27, Issue 5, May 1978 Page(s):408 - 413
 Digital Object Identifier 10.1109/TC.1978.1675120
[AbstractPlus](#) | [Full Text: PDF\(3402 KB\)](#) [IEEE JNL](#)
[Rights and Permissions](#)
-
- ☐ **21. Tolerating late memory traps in dynamically scheduled processors**
 Qiu, X.; Dubois, M.;
[Computers, IEEE Transactions on](#)
 Volume 53, Issue 6, June 2004 Page(s):732 - 743
 Digital Object Identifier 10.1109/TC.2004.18
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(1064 KB\)](#) [IEEE JNL](#)
[Rights and Permissions](#)
-
- ☐ **22. Benchmarking the MIT LL HPCMP DHPI System**
 Reuther, A.; Funk, A.; Kepner, J.; McCabe, A.; Arcand, W.; Currie, T.; Hubbell, M.; Michaleas, P.;
[DoD High Performance Computing Modernization Program Users Group Conference, 2007](#)
 18-21 June 2007 Page(s):310 - 316
 Digital Object Identifier 10.1109/HPCMP-UGC.2007.12
[AbstractPlus](#) | [Full Text: PDF\(330 KB\)](#) [IEEE CNF](#)
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-
- ☐ **23. Stream Scheduling: A Framework to Manage Bulk Operations in a Memory Hierarchy**
 Das, Abhishek; Dally, William J.;
[Parallel Architecture and Compilation Techniques, 2007. PACT 2007, 16th International Conference on](#)
 15-19 Sept. 2007 Page(s):405 - 405
 Digital Object Identifier 10.1109/PACT.2007.4336233
[AbstractPlus](#) | [Full Text: PDF\(69 KB\)](#) [IEEE CNF](#)
[Rights and Permissions](#)
-
- ☐ **24. Multiprocessor system-on-chip data reuse analysis for exploring customized memory hierarchies**
 Issenin, I.; Brockmeyer, E.; Durinck, B.; Dutt, N.;
[Design Automation Conference, 2006 43rd ACM/IEEE](#)
 24-28 July 2006 Page(s):49 - 52
[AbstractPlus](#) | [Full Text: PDF\(2408 KB\)](#) [IEEE CNF](#)
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-
- ☐ **25. Multi-level on-chip memory hierarchy design for embedded chip multiprocessors**
 Ozturk, O.; Kandemir, M.; Irwin, M.J.; Tosun, S.;
[Parallel and Distributed Systems, 2006. ICPADS 2006, 12th International Conference on](#)
 Volume 1, 12-15 July 2006 Page(s):8 pp.
 Digital Object Identifier 10.1109/ICPADS.2006.66
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